REMARKS

Claims 1-8 are pending in the application. Claims 7-8 are allowed. Claims 1-3 and 5-6 are rejected. Claim 4 is objected to for being dependent on a rejected base claim but would be allowable if rewritten into independent form.

Claims 1-2 and 5-6 are rejected under 35 USC § 103 as being unpatentable over US patent 6,009,028 (referred to as "Akiyama") in view of US patent 6,499,119 (referred to as "Orita"). The Office Action indicates Akiyama discloses all that is claimed except "the step of rendering a decision that, when the read-out logical value and the written logical value do not coincide with each other" [sic]; that Orita discloses this missing step; and that it would have been obvious to combine these teachings.

Applicants amend claims 1 and 5 and request reconsideration. Akiyama and Orita, either individually or in combination, do not disclose or suggest all steps of these claims.

Akiyama discloses a device for testing a designated region of conventional multi-bit semiconductor memory such as that described in the background section of the present application. Orita discloses testing storage devices like conventional semiconductor memory and does not disclose anything beyond what is disclosed in Akiyama that is relevant to the present invention.

In contrast to what these references disclose, the method of claim 1 comprises:

> writing a predetermined logical value in memory cells constituting each of blocks of a memory having a block function by which memory cells in a block are erased en bloc and made rewritable;
>
> reading out the written logical value from the memory cells in each block;
>
> rendering a decision that, when the written logical value and the read-out logical value do not coincide with each other, such memory cell is a failure memory cell; and
>
> discontinuing the test of such block when the number of failure memory cells in a block being now tested reaches a predetermined number indicating repair of the memory is impossible by substitution of spare memory components.

Neither reference discloses or suggests testing memory cells constituting blocks of a memory having a block function (which has been clarified by amendment) and neither reference discloses discontinuing testing a block when the number of failure memory cells in that block reach a predetermined number indicating repair of the memory is not possible by substitution of spare memory components.

Similar reasons apply to claim 5. All of the other rejected claims depend from either claim 1 or claim 5 and add further limitations.

CONCLUSION

Applicants request reconsideration in view of the discussion set forth above.

Respectfully submitted,

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Certificate of Transmission

I certify that this Response to Office Action and any following materials are being transmitted by facsimile on November 25, 2003 to the U.S. Patent and Trademark Office at telephone number (703) 746-7239.

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